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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	William J. Dally and John W. Poulton		
Application No.:	09/557,640	Group:	2665
Filed:	April 25, 2000	Examiner:	Thien D. Tran
Confirmation No.:	9254		
For:	CLOCK MULTIPLYING DELAY-LOCKED LOOP FOR DATA COMMUNICATIONS		

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RESPONSE

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This Response is being filed with a Request for Continued Examination in response to the Final Office Action mailed from the U.S. Patent and Trademark Office on February 12, 2004 in the above-identified application.

Applicant thanks Examiner Tran for a helpful telephone interview with an inventor, Dr. Dally, and the undersigned and for a follow up telephone conversation with the undersigned. Following are points raised during those discussions, and it is believed that the following comments support allowance of all claims.

Claim 1 can be compared to Figure 5 of the present application as follows:

1. A clock multiplier comprising:

a delay line (142) which provides a multiplied clock (bclk);

a clock multiplexer (141) which applies as an input (117) to the delay line (142), at respective times, the multiplied clock (bclk) and a reference clock (rclk); and

a delay adjustment circuit including a proportional phase comparator (147) which adjusts delay in the delay line (142) based on a direct phase comparison of the reference clock (rclk) and of the multiplied clock (bclk) .

Note that the same multiplied clock bclk is applied to both the multiplexer 141 and to the phase comparator 147. The phase comparator is included in a circuit that loops back to adjust the delay of the delay line 142.

Li et al. also has a delay line that provides a multiplied clock CLK_{D2}. It also includes a multiplexer 216 that applies as an input to the delay line, at respective times, the mutliplied clock CLK_{D2} and a reference clock CLK_{REF}. Li et al. also includes a phase comparator 202, though not a proportional phase comparator, that adjusts delay in the delay line. However, the comparator 202 does not make a "direct phase comparison of the reference clock and the multiplied clock." The signal CLK_{D2} (which is the same as CLK_{OUT}) is divided down to provide a signal CLK^*_{OUT} that is applied to the phase comparator 202. CLK_{D2} is not applied directly to the phase comparator but rather is first divided down.

The Examiner suggested that the signal CLK^*_{OUT} might be considered a multiplied clock with a multiplier of 1. It is first submitted that a multiplier of 1 does not result in a "multiplied clock" as that term must be interpreted in view of the specification. Further, claim 1 makes three references to a single "multiplied clock": at the output of the delay line, at the input to the multiplexer, and at the input to the phase comparator. If CLK^*_{OUT} is considered to be the multiplied clock, then it fails to meet the other requirements of the claim that the multiplied clock be at the output of the delay line and at the input of the multiplexer. If one more correctly considers CLK_{D2} to be the multiplied clock at the output of the delay line and at the input of the

multiplexer, that multiplied clock is not directly compared to the reference clock in the phase comparator 202 as required in the claims.

All independent claims of the application similarly distinguish Li et al.

It is noted in the Office Action at page 4 that the Examiner sees the phase difference output from the comparator as a phase offset. It is respectfully submitted that a phase offset is a characteristic of a comparator well known to those skilled in the art that is distinct from the phase difference output from the comparator.

Information Disclosure Statement

An Information Disclosure Statement (IDS) is being filed concurrently herewith to reference another application of the same assignee and the references cited in that application. Entry of the IDS is respectfully requested.

CONCLUSION

In view of the above remarks, it is believed that all claims are in condition for allowance, and it is respectfully requested that the application be passed to issue. If the Examiner feels that a telephone conference would expedite prosecution of this case, the Examiner is invited to call the undersigned.

Respectfully submitted,

HAMILTON, BROOK, SMITH & REYNOLDS, P.C.

By _____
James M. Smith
Registration No. 28,043
Telephone: (978) 341-0036
Facsimile: (978) 341-0136

Concord, MA 01742-9133
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